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10EC077

M.Tech. Degree Examination, January 2013
Synthesis and Optimization of Digital Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Explain in detail, microelectronics design styles. **(08 Marks)**

b. What are the different phases involved in the design of microelectronics circuits. Briefly explain each of them. **(06 Marks)**

c. Consider the function $f = ab + bc + ac$, compute an expansion on orthonormal basis. (given $\phi_1 = ab$ and $\phi_2 = \bar{a} + \bar{b}$) verify ϕ_1 and ϕ_2 are orthonormal. **(06 Marks)**

2 a. Compute the longest path weight of the graph shown below using LIAO – WONG algorithm. Show the graphs in each step. **(08 Marks)**

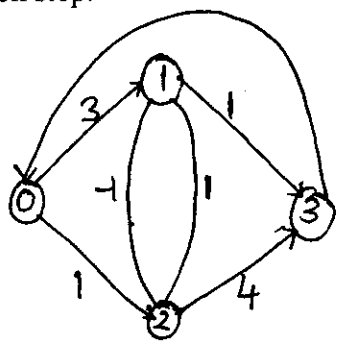

Fig. Q2(a)

b. For the vertex /edge incidence matrix shown. Find exact/minimum cover using EXACT – COVER algorithm. With the pseudo code for the same.

$$A_1 = \begin{bmatrix} 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 1 & 1 & 0 \end{bmatrix}$$ **(12 Marks)**

3 a. Draw the mealy state machine to detect two or more consecutive 1's in an input data stream. Write the VHDL behavioral model for the same. **(08 Marks)**

b. With suitable examples, briefly explain the various data flow based transformations. **(12 Marks)**

4 a. For the function $f = ab + ac + \bar{a}$, compute all prime implicates using SCC operator. **(08 Marks)**

b. Consider the function $f(abc) = \Sigma m\,(0, 1, 2, 4) + d\,(6)$. Find expanded cover which is prime and minimal with respect to single implicant containment. **(12 Marks)**

5 a. With suitable example, explain ill – posed and well – posed constraints. **(06 Marks)**

b. Write the pseudo code for Force – directed scheduling algorithm for minimum – latency scheduling problem under resource constaints. Briefly give the comments. **(07 Marks)**

c. What is the need of loop folding? With suitable sequencing graph, explain loop folding. **(07 Marks)**

6 a. For the function G_x = ace + bce + de + f, G_S = cde + b, and auxiliary function G_{aux} = ace + bce + de + f + cde + b. write cube –variable matrix and obtain prime rectangle. Show extraction of ce and draw extraction of single – implicant sub expression. **(10 Marks)**

b. Consider the logic network shown below, determine topological critical path for vertices with zero slack. Assume the input data ready times of $t_a = 0$ and $t_b = 10$ and propagation delay of internal vertices be $d_g = 3$, $d_h = 8$, $d_m = 1$, $d_k = 10$, $d_L = 3$ dn = 5, $d_p = 2$, $d_q = 2$, $d_x = 2$, $d_y = 3$. Give the relations used. **(10 Marks)**

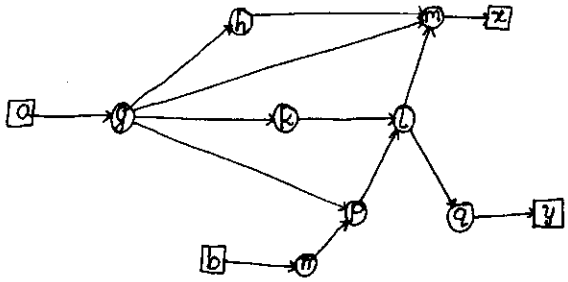

Fig. Q6(b)

7 a. For the state table shown, draw the mealy state diagram. List the compatible and incompatible pairs. Find the maximal classes of compatible states. Draw the minimum state diagram. **(10 Marks)**

Input	State	Next state	Output
0	S_1	S_3	1
1	S_1	S_5	*
0	S_2	S_3	*
1	S_2	S_5	1
0	S_3	S_2	0
1	S_3	S_1	1
0	S_4	S_4	0
1	S_4	S_5	1
0	S_5	S_4	1
1	S_5	S_1	0

b. What is the goal of FSM decomposition? With the help of figures, explain the different types of FSM(Finite State Machine) decomposition. Also explain the factorization. **(10 Marks)**

8 a. Explain briefly TREE – BASED covering. **(06 Marks)**

b. List and explain the types of simulators. **(06 Marks)**

c. With neat block diagram, explain built–in–self–test (BIST) architecture. **(08 Marks)**

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